UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/417,016	10/12/1999	SHIGEHIRO MASUJI	P63935US0	6885

7590 09/08/2004

JACOBSON PRICE HOLMAN & STERN
PROFESSIONAL LIMITED LIABILITY COMPANY
400 SEVENTH STREET N W
WASHINGTON, DC 20004

EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/417,016	MASUJI ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-20 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-20 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 3-26-2004 is entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12, 14 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al. (US Patent 6,069,609) in view of Sakano (US Patent # 5,144,456).

As to claim 10, Ishida et al. teaches an apparatus for processing a video signal comprising a pattern generator (dither pattern generator 13 shown in figure I 0A) to generate a plurality of dither pattern signals, carrying positional data indicating locations of dither coefficients, a coefficient generator to generate a dither coefficient signal carrying the dither coefficients arranged in a matrix (2x2 dither matrices, column 20, lines 51-57) for each gradation level of an input video signal (28 ranges within 256-shade grayscale shown in figure 18) in response to one of the pattern signal, and an adder (adder 12, figure 10A, column 10, line 50) to add the coefficient signal to the input video signal (column 12, lines 61-62), thus outputting a video signal to be supplied

to the display panel (PDP 21 shown in figure 11), wherein the adder adds the coefficient signal to the input video signal at gradation levels equal to or lower than a predetermined level (optimum value of A according to 256-shade grayscale shown in figure 19, threshold for each dither pattern is zero to 10, column 12, lines 66-67). Ishida et al teaches weighting ring applied to each dither coefficient (column 13, lines 57-65). However Ishida et al fails to expressly teach the lower the gradation level, and the larger the weighing.

Sakano teaches a relatively large weighting factor is given the gradation level of a pixel close to the pixel of concern, and a relatively small weighting factor is given the gradation level of a pixel far from the pixel of concern (column 7, lines 43-47).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the weighted factor as taught by Sakano in the image processor disclosed by Ishida et al. because this would provide an image processing apparatus capable of eliminating a background contamination from a readout image signal without affecting a signal component of a real image contained in the readout image signal (column 1, lines 48-51).

As to claim 11, Ishida et al. discloses an apparatus for processing a video signal (image processing device, abstract) comprising a generator (dither pattern generator 13 shown in figure I0A) to generate a plurality of dither coefficient signals, each coefficient signal carrying dither coefficients arranged in a matrix (2x2 dither matrices, column 20, lines 51-57); an adder (adder 12, figure 10A, column 10, line 50) to add one of the coefficient signals to signal components at predetermined gradation levels of the input

video signal (256-shade grayscale as shown in figure 19), thus output a video signal. Ishida et al. does teach 8-bit input signal for each color RGB (column 8, lines 2-3, column 11, lines 28-29), and grayscale levels in figure 19, dither pattern generator 23 shown in figure 11 receiving RGB input signals but Ishida et al. fails to expressly teach a detector to detect color gradation levels of an input video signal.

As to claim 12, wherein each coefficient signal carrying positive and negative coefficients (+A and -A, figure 15), the sum total of the coefficients being zero (sum A-A-A+A is zero, figure 15).

As to claim 14, wherein weighting is applied to the dither coefficients carried by each pattern signal (figure 19 show optimum value of A depending on gray-scale levels). However, Ishida et al. fails to expressly teach the lower the gradation the larger the weighting. Note that Ishida et al. teaches dither value to deal with a shade that may easily flicker and lighting order of subframes (column 15, lines 36-39), that human eye senses flicker at low brightness levels, at high brightness levels, the subframes to be turned ON vary little (column 19, lines 7-10).

As to claim 30, Ishida et al. teaches the step of applying weighting to the dither coefficients carried by each pattern signal (figure 19 show optimum value of A depending on gray-scale levels), but fails to teach the lower the gradation, the larger the weighting. Note that Ishida et al. teaches dither value to deal with a shade that may easily flicker and lighting order of subframes (column 15, lines 36-39), that human eye senses flicker at low brightness levels, at high brightness levels, the subframes to be turned ON vary little (column 19, lines 7-10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13, 15-20, 28, 29, and 31-33 are rejected under 35 USC 102 (e) as being unpatentable over Ishida et al. (US Patent # 6,069,609).

As to claim 13, Ishida et al. teaches an apparatus for processing a video signal comprising: a coefficient generator to generate a plurality of dither coefficient pattern signals (dither pattern generator shown in figure I0A) according to color gradation levels (8-bit input signal for each color RGB, column 8, lines 2-3, gray scale levels in figure 19), a selector (selector 32/34 shown in figure 27, column 17, lines 20-22) to select one of the dither coefficient from each pattern signal with respect to each dot matrix, an adjuster to adjust the dither coefficients carried by the output pattern signal so that the sum total of the dither coefficients is zero (since sum A-A-A+A is zero , figure 15, column 11, lines 4-5, therefore adjuster to adjust the dither coefficients is inherent) and the dither pattern generator 13 selects one of the dither patterns prepared in advance (column 10, lines 47-49), an adder (adder 12, figure 10A, column 10, line 50) to add the dither coefficient-adjusted pattern signal to the input video

signal, thus outputting a video signal carrying the data to be supplied to the display panel (PDP 21 shown in figure I1).

As to claim 15, wherein the selector selects one dither coefficient for each predetermined unit of the data carried by the video signal or according to locations of the pixels on the display panel selector selects one of the dither types, column 22, lines 50-51).

As to claim 16, wherein the dither coefficients are arranged in an (nxm) matrix, where n and m being a positive integer larger than zero (figure 17 where n=m=2).

As to claim 17, wherein each pattern signal carries an even number of the coefficients addition of the coefficients in each of the two groups yielding zero when the coefficients are divided in the two groups (figure 15 shows groups +A and -A).

As to claim 18, Ishida et al. fails to teach dither matrix wherein each pattern signal carries an odd number of the coefficients, the coefficient located at the center of the matrix being zero. However, since figure 15 shows the sum of dither coefficients being zero and Ishida et al. discloses that any matrix is employable (column 13, lines 1-2), it is inherent in the art , in case of a (nxm) matrix where n is different from m, to easily determine value of dither coefficient at the center of matrix to keep sum of all dither coefficients being zero.

As to claim 19, the apparatus according to claim 16, where n and m are equal to each other figure 15 where n=m=2).

As to claim 20, wherein each pattern signal carries the same number of the positive and the negative coefficients (figure 15 shows groups +A and -A).

As to claim 28, Ishida et al. teaches a method of processing a video signal comprising the steps of generating a plurality of dither pattern signals (dither pattern generator 13 shown in figure l0A generating dither pattern signals), each pattern signal carrying positional data indicating locations of dither coefficients on pixels arranged in a matrix on a display panel, generating a dither coefficient signal (2x2 dither matrices, column 20, lines 51-57) carrying the dither coefficients arranged in a matrix for each gradation level of an input video signal in response to one of the pattern signal(28 ranges within 256-shade grayscale shown in figure 18), adding (adder 12, figure 10A, column 10, line 50) the dither coefficient signal to the input video signal (column 12, lines 61-62), thus outputting a video signal to be supplied to the display panel (PDP 21 shown in figure 11) wherein the addition step comprises the step of adding the coefficient signal to the input video signal at gradation levels equal to or lower than a predetermined level (optimum value of A according to 256-shade grayscale shown in figure 19, threshold for each dither pattern is zero to 10, column 12, lines 66-67) and said display whose original number of shades is represented with m bits and is equal or less than 2m in order to artificially increase the number of shades.

As to claim 29, Ishida et al. teaches a method of processing a video signal comprising the steps of generating a plurality of dither coefficient pattern signals (dither pattern generator shown in figure l 0A) according to color gradation levels (8-bit input signal for each color RGB, column 8, lines 2-3, gray scale levels in figure 19), selecting one of the dither coefficient from each pattern signal with respect to each dot matrix (selector 32/34 shown in figure 27, column 17, lines 20-22) adjusting the dither

coefficients carried by the output pattern signal so that the sum total of the dither coefficients is zero (sum A-A-A+A is zero , figure 15, column 11, lines 4-5) and the dither pattern generator 13 selects one of the dither patterns prepared in advance (column 10, lines 47-49), adding the dither coefficient-adjusted pattern signal to the input video signal (adder 12, figure 10A, column 10, line 50, column 12, lines 61-62) , thus outputting a video signal carrying the data to be supplied to the display panel (PDP 21 shown in figure 11).

As to claim 31, wherein the selection step comprises the step of selecting one dither coefficient for each predetermined unit of the data carried by the video signal or according to locations of the pixels on the display panel (selector selects one of the dither types, column 22, lines 50-51). As to claim 32, wherein the pattern signals are generated so that each pattern signal carries an even number of the coefficients, addition of the coefficients in each of the two groups yielding zero when the coefficients are divided into the two groups, both groups including the same number of the coefficients (figure 15 shows groups +A and -A).

As to claim 33, Ishida et al. fails to teach dither matrix wherein each pattern signal carries an odd number of the coefficients, the coefficient located at the center of the matrix being zero. However, since figure 15 shows the sum of dither coefficients being zero and Ishida et al. discloses that any matrix is employable (column 13, lines 1-2), it is inherent in the art, in case of a (nxm) matrix where n is different from m, to easily determine value of dither coefficient at the center of matrix to keep sum of all dither coefficients being zero.

Response to arguments

Applicant's arguments filed 3-28-2004 have been fully considered but they are not persuasive. The applicant argued that the prior art does not teach "the lower the gradation level, the larger the weighting". Examiner agrees with the applicant but has found a new piece of art that teaches a relatively large weighting factor is given the gradation level of a pixel close to the pixel of concern, and a relatively small weighting factor is given the gradation level of a pixel far from the pixel of concern (column 7, lines 43-47) which can be interpreted as the lower the gradation level, the larger the weighting. Furthermore, the applicant argued that the prior art does not teach adding coefficient signal to the input signal at gradation levels equal to or lower than a predetermined level. Examiner disagrees with the applicant because the prior art teaches said display whose original number of shades is represented with m bits and is equal or less than 2m in order to artificially increase the number of shades (column 25, lines 43-45). The applicant needs to amend the claims to really teach away from the pertinent prior art of record.

Conclusion

The prior art made of record but not relied upon is pertinent to Applicant's disclosure:

US Patent Choi et al. 5,495,346

US Patent Barkans et al. 5,905,504

US Patent Rao et al. 5,640,249

US Patent Shigeta 6,008,793

US Patent Priem et al. 5,734,369

Reference Choi et al. is made of record as it discloses an element generator for a dither matrix.

Reference Barkans et al. is made of record as it discloses a system and method for dithering and quantizing image data.

Reference Rao et al. is made of record as it discloses an image processing apparatus using derived ordered dither matrix.

Reference Shigeta is made of record as it discloses a drive apparatus comprising a dithering circuit.

Reference Priem et al. is made of record as it discloses a method and apparatus for dithering images .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Richard Hjerpe, can be reached on (703) 305-4709.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office Whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 8-27-2004

RICHARD HJERPE 9/7/04
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600